

CURRICULUM VITAE
ALI ASGHAR OROUJI

PERSONAL DETAILS

- First Name: **Ali Asghar**
- Surname: **Orouji**
- Sex: Male
- Nationality: Iranian

QUALIFICATIONS

Ph.D.

Electronics Engineering from Indian Institute of Technology-Delhi.

M.Sc.

Master of Electronics Engineering from Iran University of Science & Technology.

B.Sc.

Electronics Engineering from Iran University of Science & Technology.

A Levels

Maths, Physics, Chemistry from Dehkhoda High School of Karaj.

EDUCATION

2003-2006 Indian Institute of Technology-Delhi New Delhi, India

Ph. D., Electronics Engineering.
Graduated with honors degree.

1989-1992 Iran University of Science & Technology (IUST) Tehran, Iran

M.Sc., Master of Electronics.
Graduated with honors degree.

1984-1989 Iran University of Science & Technology (IUST) Tehran, Iran

B.Sc., Electronics Engineering
Graduated with honors degree.

1980-1984 Dehkhoda High School Karaj, Iran

A Levels in Maths, Physics, Chemistry.

EXPERIENCE

- * Faculty Member of Electrical Engineering Department, Semnan University from 1992-Present
- * Head of Electronics Group from 2008-Present.
- * Professor from 2014-Present.
- * Senior Member, *IEEE*.
- * Teaching many courses in Electrical Engineering Department.
- * Supervisor of more than hundred undergraduate students.
- * Supervisor of more than twenty M. Sc. students.
- * Supervisor of 7 Ph.D. students.
- * Publishing more than hundred papers in International Journals and conferences.
- *Setting up of Pulse Technique laboratory (in 1993).
- *Setting up of Electronics III laboratory (in 1994).
- * Papers reviewer for International Journals/Conferences such as *IEEE* Transaction on Electron Device, Solid State Electronics ...

BOOK PUBLICATION

- “Wave Generation and Shaping”
Book published (in Persian) in Tehran, Iran, Sep. 2001.
Second edition published in Tehran, Iran, Sep. 2011.

BOOKLET & MANUAL PUBLICATIONS

“Television Systems”

Booklet published (in Persian) in Tehran, Iran, Sep. 1994.

“Electronics III Principles”

Booklet published (in Persian) in Tehran, Iran, Sep. 1993.

“Communication Circuits”

Booklet published (in Persian) in Tehran, Iran, Feb. 1996.

“Pulse Technique laboratory”

Manual published (in Persian) in Tehran, Iran, Sep. 1993.

“Electronics III laboratory”

Manual published (in Persian) in Tehran, Iran, Sep. 1994.

RESEARCH PLANS

- Shot Noise in Bipolar Junction Transistors, June 1995, Semnan Iran.
- Short Channel effects Technique in Nano MOSFETs, Jan. 2008, Semnan Iran.
- Electron Scattering in Nano Field Effect Trsistors, Nov. 2009, Semnan Iran.
- Self-heating in Nano Field Effect Transistor at Silicon on Insulator Technology, June 2011, Semnan Iran.

JOURNAL & MAGAZINE PUBLICATIONS

1. M. K. Anvarifard and Ali. A. Orouji, "Evidence for Enhanced Reliability in a Novel Nanoscale Partially-Depleted SOI MOSFET," *IEEE Trans. on Device and Materials Reliability*, 2014.
2. Ali A. Orouji and M. K. Anvarifard, " Novel Reduced Body Charge Technique in Reliable Nanoscale SOI MOSFETs for Suppressing the Kink Effect," *Superlattices and Microstructures*, pp. 111-125, August 2014.
3. Ali A. Orouji, M. Eslamijam, and M. Nejati, "A Novel SOI MESFET by Reducing the Electric Field Crowding for High Voltage Applications," *Superlattices and Microstructures*, pp. 11-24, August 2014.
4. H. Shahnazarisani, Ali A. Orouji, and M. K. Anvarifard, "A novel SOI MESFET by π -shaped gate for improving the driving current," *Journal of Computational Electronics*, March 2014.
5. M. Charmi, H. R. Mashayekhi, and Ali A. Orouji, "The impact of high-k gate dielectric and FIBL on performance of nano DG-MOSFETs with underlapped source/drain regions," *Journal of Computational Electronics*, pp. 307-312, March 2014.

6. M. K. Anvarifard and Ali A. Orouji, "Improvement of Electrical Properties in a Novel Partially Depleted SOI MOSFET With Emphasizing on the Hysteresis Effect," *IEEE Trans. on Electron Devices*, Vol. 60, pp. 3310-3317, October 2013.
7. M. Zareiee, A. Dideban, and Ali A. Orouji, "Safety analysis of discrete event systems using a simplified Petri net controller," *ISA Transactions*, Vol. 53, pp. 44-49, 2014.
8. Z. Ramezani and Ali A. Orouji, "A silicon-on-insulator metal–semiconductor field-effect transistor with an L-shaped buried oxide for high output-power density," *Materials Science in Semiconductor Processing*, Volume 19, pp. 124-129, March 2014.
9. M. Rahimian, Ali A. Orouji, and A. Aminbeidokhti, "A novel deep submicron SiGe-on-insulator (SGOI) MOSFET with modified channel band energy for electrical performance improvement," *Current Applied Physics*, Volume 13, Issue 4, pp. 779-784, June 2013.
10. Ali A. Orouji and M. K. Anvarifard, "SOI MOSFET with an insulator region (IR-SOI): A novel device for reliable nanoscale CMOS circuits," *Materials Science and Engineering: B*, Volume 178, Issue 7, pp. 431-437, April 2013.
11. M. Charmi, Ali A. Orouji, and H. R. Mashayekhi, "Design considerations of underlapped source/drain regions with the Gaussian doping profile in nano-double-gate MOSFETs: A quantum simulation," *Materials Science in Semiconductor Processing*, Volume 16, Issue 2, pp. 311-317, April 2013.
12. M. Rahimian and Ali A. Orouji, "A novel nanoscale MOSFET with modified buried layer for improving of AC performance and self-heating effect," *Materials Science in Semiconductor Processing*, Volume 15, Issue 4, pp. 445-454, August 2012.
13. M. K. Anvarifard and Ali A. Orouji, "Improvement of self-heating effect in a novel nanoscale SOI MOSFET with undoped region: A comprehensive investigation on DC and AC operations," *Superlattices and Microstructures*, Volume 60, pp. 561-579 August 2013.
14. M. Mehrad and Ali A. Orouji, "Injected charges in partial SOI LDMOSFETs: A new technique for improving the breakdown voltage ," *Superlattices and Microstructures*, Volume 57, pp. 77-84 May 2013.
15. M. Rahimian and Ali A. Orouji, "Investigation of the Electrical and Thermal Performance of SOI MOSFETs with Modified Channel Engineering," *Materials Science in Semiconductor Processing*, Volume 16, Issue 5, pp. 1248-1256 October 2013.
16. Ali A. Orouji, Z. Ramezani, P. Keshavarzi, and A. Aminbeidokhti, "A novel high frequency SOI MESFET by modified gate capacitances," *Superlattices and Microstructures*, Volume 61, pp. 69-80 September 2013.
17. A. Abbasi and Ali A. Orouji, "A silicon/indium arsenide source structure to suppress the parasitic bipolar-induced breakdown effect in SOI MOSFETs," *Materials Science in Semiconductor Processing*, Volume 16, Issue 6, pp. 1821-1827, December 2013.
18. M. K. Anvarifard and Ali A. Orouji, "Voltage difference engineering in SOI MOSFETs: A novel side gate device with improved electrical performance,"

- Materials Science in Semiconductor Processing*, Volume 16, Issue 6, pp. 1672-1678 December 2013.
19. M. Zareiee, A. Dideban, Ali A. Orouji, and H. R. Solymannpour, "Simplification of a Petri Net Controller in industrial systems by using an optimization algorithm," *International Journal of Industrial Engineering & Production Research*, pp.59-70, March 2013.
 20. Ali A. Orouji, R. Esmailnezhad, and M. Rahimian, "A novel vertical stepped doping poly-Si TFT (VSD-TFT) for leakage current improvement," *Superlattices and Microstructures*, Volume 63, pp. 18-28, November 2013.
 21. M. Mehrad and Ali A. Orouji, " A novel high voltage lateral double diffused metal oxide semiconductor (LDMOS) device with a U-shaped buried oxide feature," *Materials Science in Semiconductor Processing*, Volume 16, Issue 6, pp. 1977-1981, December 2013.
 22. A. Aminbeidokhti, Ali A. Orouji, and M. Rahimian, " High-Voltage and RF Performance of SOI MESFET Using Controlled Electric Field Distribution," *IEEE Trans. on Electron Devices*, pp. 2842-2845, October 2012.
 23. Ali A. Orouji and M. Mehrad, "Breakdown voltage improvement of LDMOSs by charge balancing: An inserted P-layer in trench oxide (IPT-LDMOS)," *Superlattices and Microstructures*, Volume 51, Issue 3, pp. 412-420, March 2012.
 24. Ali A. Orouji and M. Rahimian, "Leakage current reduction in nanoscale fully-depleted SOI MOSFETs with modified current mechanism," *Current Applied Physics*, Volume 12, Issue 5, pp. 1366-1371, September 2012.
 25. M. Mehrad and Ali A. Orouji, "New trench gate power MOSFET with high breakdown voltage and reduced on-resistance using a SiGe zone in drift region," *Current Applied Physics*, Volume 12, Issue 5, pp. 1340-1344, September 2012.
 26. S. M. Razavi, Ali A. Orouji, and S. E. Hosseini, "Recessed p-buffer layer SiC MESFET: A novel device for improving DC and RF characteristics," *Materials Science in Semiconductor Processing*, Volume 15, Issue 5, pp. 516-521, October 2012.
 27. Ali A. Orouji, H. R. Mashayekhi, and M. Charmi, "Design considerations of source and drain regions in nano double gate MOSFETs," *Materials Science in Semiconductor Processing*, Volume 15, Issue 5, pp. 572-577, October 2012.
 28. H. Elahipanah, Ali A. Orouji, "Gain improvement and microwave operation of 4H-SiC MESFET with a new recessed metal ring structure," *Microelectronics Journal*, Volume 43, Issue 7, pp. 466-472, July 2012.
 29. A. Aminbeidokhti, Ali A. Orouji, S. Rahmaninezhad, and M. Ghasemian, "A Novel High-Breakdown-Voltage SOI MESFET by Modified Charge Distribution," *IEEE Trans. on Electron Devices*, pp. 1255-1262, May 2012.
 30. A. Aminbeidokhti and Ali A. Orouji, "A new double-recessed 4H-SiC MESFET with superior RF characteristics," *International Journal of Electronics*, Vol.100, Issue 2, 2013.
 31. Ali A. Orouji and M. Mehrad, "The Best Control of Parasitic BJT Effect in SOI-LDMOS with SiGe Window under Channel," *IEEE Trans. on Electron Devices*, 2012.

32. M. Mehrad and Ali A. Orouji, "A new nanoscale and high temperature field effect transistor: Bi level FinFET," *Physica E- Low-dimensional Systems and Nanostructures*, pp. 654-658, December 2011.
33. A. Aminbeidokhti and Ali A. Orouji, "A novel 4H-SiC MESFET with modified channel depletion region for high power and high frequency applications," *Physica E- Low-dimensional Systems and Nanostructures*, pp. 708-713, December 2011.
34. M. Rahimian and Ali A. Orouji, "Nanoscale SiGe-on-insulator (SGOI) MOSFET with graded doping channel for improving leakage current and hot-carrier degradation," *Superlattices and Microstructures*, pp. 667-679, December 2011.
35. M. Mehrad and Ali A. Orouji, "A New Rounded Edge Fin Field Effect Transistor (RE-FinFET) for Improving Self-heating Effects," *Japanese Applied Physics*, vol. 50, pp. 114503 (6 pages), December 2011.
36. Ali A. Orouji and A. Aminbeidokhti, "A novel double-recessed 4H-SiC MESFET with partly undoped space region," *Superlattices and Microstructures*, pp. 680-690, December 2011.
37. Ali A. Orouji, S. M. Razavi, S. E. Hosseini, and H. Amini Moghadam, "Investigation of the Novel Attributes in Double Recessed Gate SiC MESFETs at Drain Side," *Semiconductor Science and Technology*, 2011.
38. Ali A. Orouji and M. Rahimian, "Dual Material Insulator SOI-LDMOSFET: A Novel Device for Self-Heating Effect Improvement," *Physica E- Low-dimensional Systems and Nanostructures*, pp. 333-338, October 2011.
39. Ali A. Orouji, E. Jamali, and P. Keshavarzi, "A Novel Partial SOI LDMOSFET with a Trench and Buried P Layer for Breakdown Voltage Improvement," *Superlattices and Microstructures*, pp. 449-460, November 2011.
40. H. Amini Moghadam and Ali A. Orouji, "Design and Performance Considerations of novel 4H-SiC MESFET with a p-type Pillar for Increasing Breakdown Voltage," *Physica E- Low-dimensional Systems and Nanostructures*, pp. 1779-1782, August 2011.
41. E. Jamali, Ali A. Orouji, P. Keshavarzi, and H. Amini Moghadam, "A New Partial SOI LDMOSFET with Modified Buried Oxide Layer for Improving Self Heating and Breakdown Voltage," *Semiconductor Science and Technology*, 2011.
42. M. Zareiee, A. Dideban, and Ali A. Orouji, "Time Management Approach on a Discrete Event Manufacturing System Modeled by Petri Net," *International Journal of Industrial Engineering & Production Research*, pp.115-121, June 2011.
43. A. Naderi, P. Keshavarzi, and Ali A. Orouji, "LDC-CNTFET: A Carbon Nanotube Field Effect Transistor with Linear Doping Profile Channel," *Superlattices and Microstructures*, pp. 145-156, August 2011.
44. Z. Arefinia and Ali A. Orouji, "Novel Attributes in the characteristics and short channel effects of double gate carbon nanotube field-effect transistors," *Esteghlal Magazine*, 2011 (in Persian).
45. Ali A. Orouji, H. Amini Moghadam, and A. Dideban, "Double Window Partial SOI-LDMOSFET: A Novel Device for Breakdown Voltage Improvement," *Physica E- Low-dimensional Systems and Nanostructures*, 2010.

46. H. Elahipanah and Ali A. Orouji, "A 1300 V–0.34 $\Omega\cdot\text{cm}^2$ Partial SOI LDMOSFET with Novel Dual Charge Accumulation Layers," *IEEE Trans. on Electron Devices*, 2010.
47. M. Mehrad and Ali A. Orouji, "Partially Cylindrical Fin Field Effect Transistor: A Novel Device for Nanoscale Applications," *IEEE Trans. on Device and Materials Reliability*, 2010.
48. Ali A. Orouji and H. Elahipanah, "A novel Nanoscale 4H-SiC On Insulator MOSFET Using Step Doping Channel," *IEEE Trans. on Device and Materials Reliability*, 2010.
49. Ali A. Orouji and S. A. Ahmadmiri, "Novel Attributes and Design Considerations of Source and Drain Regions in Carbon Nanotube Transistors," *Physica E- Low-dimensional Systems and Nanostructures*, 2010.
50. H. Elahipanah and Ali A. Orouji, "A Novel Step-Doping Fully-Depleted Silicon-on-Insulator Metal–Oxide–Semiconductor Field-Effect Transistor for Reliable Deep Sub-micron Devices," *Japanese Applied Physics*, vol. 48, pp. 114503 (5 pages), Nov. 2009.
51. Ali A. Orouji, Samane Sharbati, and M. Fathipour, "A New Partial-SOI LDMOSFET With Modified Electric Field for Breakdown Voltage Improvement," *IEEE Trans. on Device and Materials Reliability*, pp. 449-453, Sep. 2009.
52. Ali A. Orouji, Sara Heydari, and M. Fathipour, "Double step buried oxide (DSBO) SOI-MOSFET: A proposed structure for improving self-heating effects," *Physica E- Low-dimensional Systems and Nanostructures*, pp. 1665-1668, September 2009.
53. Z. Arefinia and Ali A. Orouji, "Novel attributes in the performance and scaling effects carbon nanotube field-effect transistors with halo doping," *Superlattices and Microstructures*, pp. 535-546, June 2009.
54. Z. Arefinia and Ali A. Orouji, "Quantum Simulation Study of a New Carbon Nanotube Field-Effect Transistor with Electrically Induced Source/Drain Extension," *IEEE Trans. on Device and Materials Reliability*, Vol. 9, No. 2, pp.237 – 243, June 2009.
55. Z. Arefinia and Ali A. Orouji, "Performance and Design Considerations of a Novel Dual-Material Gate Carbon Nanotube Field-Effect Transistors: Nonequilibrium Green's Function Approach," *Japanese Applied Physics*, vol. 48, pp. 024501 (7 pages), Feb. 2009.
56. Ali A. Orouji and Z. Arefinia, "Detailed simulation study of a dual material gate carbon nanotube field-effect transistor," *Physica E- Low-dimensional Systems and Nanostructures*, pp. 552-557, Feb. 2009.
57. Z. Arefinia and Ali A. Orouji, "Novel attributes in scaling issues of carbon nano tube field-effect transistors," *Microelectronics Journal*, pp. 5-9, Jan. 2009.
58. Z. Arefinia and Ali A. Orouji, "Impact of Single Halo Implantation on the Carbon Nanotube Field-Effect Transistor: A Quantum Simulation Study," *Physica E- Low-dimensional Systems and Nanostructures*, pp. 196-201, Dec. 2008.
59. Z. Arefinia and Ali A. Orouji, "Investigation of the novel attributes of a carbon nanotube FET with high- κ gate dielectrics," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 40, pp. 3068-3071, 2008

60. M. Jagadesh Kumar and Ali. A. Orouji, "A New Gate Induced Barrier Thin Film Transistor (GIB-TFT) for Active Matrix Liquid Crystal Displays: Design and Performance Considerations," *IEEE/OSA Journal of Display Technology*, Vol.2, pp.372-377, December 2006.
61. Ali. A. Orouji and M. Jagadesh Kumar, "Leakage Current Reduction Techniques in Poly-Si TFTs for Active Matrix Liquid Crystal Displays: A Comprehensive Study," *IEEE Trans. on Device and Materials Reliability*, Vol.6, pp.315-325, June 2006.
62. M. Jagadesh Kumar and Ali. A. Orouji , "Investigation of a New Modified Source/Drain for Diminished Self-heating Effects in Nanoscale MOSFETs using Computer Simulation," *Physica E: Low-dimensional Systems and Nanostructures*, Vol. 33, Issue.1, pp.134-138, June 2006.
63. Ali A. Orouji and M. Jagadesh Kumar, "Nanoscale SOI-MOSFETs with Electrically Induced Source/Drain Extension: Novel attributes and Design considerations for Suppressed Short-channel Effects," *Superlattices and Microstructures*, Vol.39, pp. 395-405, May 2006.
64. M. Jagadesh Kumar, Ali. A. Orouji and Harshit Dhakad, "A New Dual Material Surrounding-Gate Nanoscale MOSFET: Analytical Threshold Voltage Model," *IEEE Trans. on Electron Devices*, Vol.53, pp.920-923, April 2006.
65. Ali A. Orouji and M. Jagadesh Kumar, "A New Symmetrical Double Gate Nanoscale MOSFET with Asymmetrical Side Gates for Electrically Induced Source/Drain," *Microelectronic Engineering*, Vol.83, pp.409-414, March 2006.
66. Ali A. Orouji and M. Jagadesh Kumar, "The Simulation of a New Asymmetrical Double-Gate Poly-Si with Modified Channel Conduction Mechanism for Highly Reduced OFF-state Leakage Current," *IEEE Trans. Device and Materials Reliability*, vol. 5, no. 4, pp. 675-682, Dec. 2005.
67. Ali A. Orouji and M. Jagadesh Kumar, "A New Poly-Si Triple-Gate Thin-Film Transistor (TG-TFT) with Diminished Pseudo-Subthreshold Region: Theoretical Investigation and Analysis," *IEEE Trans. Electron Devices*, vol. 52, pp. 1815-1820, Aug. 2005.
68. M. Jagadesh Kumar and Ali A. Orouji, "Two-Dimensional Analytical Threshold Voltage Model of Nanoscale Fully Depleted SOI MOSFET with Electrically Induced Source/Drain Extensions," *IEEE Trans. Electron Devices*, vol. 52, pp. 1568-1575, 2005.
69. Ali A. Orouji and M. Jagadesh Kumar, "Shielded Channel-Double Gate (SC-DG) MOSFET: A Novel Device for Reliable Nanoscale CMOS Applications," *IEEE Trans. Device and Materials Reliability*, vol. 5, no. 3, pp. 509-514, 2005.
70. Ali A. Orouji, "A Comprehensive Study of Short Channel Effects Improvement Techniques in SOI-MOSFET and a Novel Approach," IUST, 2009.
71. Ali A. Orouji, "Design and Performance Considerations of Novel Nanoscale Shielded Channel Multiple Gate MOSFET," *Iranian Journal of Engineering Sciences (IJES)*, pp. 59-67, Spring 2008.
72. Ali A. Orouji and Fattahpour, "Analysis of Different Ge-Composition Effect in SiGe Heterojunction Bipolar Transistor for photo Applications," *Magazine of Modeling in Engineering*, Semnan University.

73. Ali A. Orouji and Sara Heydari, "Design and Simulation of a Multilayer SOI-MOSFET Structure for Improving Self-Heating Effects" *Magazine of Modeling in Engineering*, Semnan University
74. Ali A. Orouji and Samane Sharbati, "Analysis and Simulation of Silicon Carbide Diode Characteristics," *Magazine of Engineering Faculty*, Semnan University, pp. 13-18, Nov. 2006. (in Persian).
75. Ali A. Orouji, "Design and Fabrication of a Voltage Controlled Resistance with Wide Dynamic Range and Low Distortion," *Magazine of Engineering Faculty*, Semnan University, pp. 55-59, Nov. 2006 (in Persian).
76. Ali A. Orouji, "Deep Level Transient Spectroscopy," *Forough Danesh Magazine*, Semnan University, pp. 9-12, 1998 (in Persian).
77. Ali A. Orouji, "Channel Access Methods in the Subnet Broadcast," *Magazine of Engineering Faculty*, Semnan University, pp. 12-14, 1998 (in Persian).
78. Ali A. Orouji, "Local Area Network," *Magazine of Engineering Faculty*, Semnan University, pp. 13-14, 1998 (in Persian).

CONFERENCE PAPERS

1. Ali A. Orouji, A. Aminbeidokhti, and M. Rahimian, "A novel GaAs MESFET with multi-recessed drift region and partly p-type doped space layer," *International Conference on Electronic Devices, Systems and Applications (ICEDSA)*, Malaysia, April, 2011.
2. Ali A. Orouji, M. Rahimian, and A. Aminbeidokhti, "A novel N-MOSFET with air gaps in gate insulator for deep submicron applications," *International Conference on Electronic Devices, Systems and Applications (ICEDSA)*, Malaysia, April, 2011.
3. H. Amini Moghadam, Ali A. Orouji, and A. Dideban, "Comparative Study of Buried Insulator Materials in LDMOSFETs," *International Conference on Computational Technologies in electrical and Electronics Engineering (SIBRICON)*, Russia, July, 2010.
4. S. A. Ahmadmiri and Ali A. Orouji, *15th International Workshop on the Physics of Semiconductor Devices (IWPSD)*, Dec. 2009.
5. H. Elahipanah and Ali A. Orouji, *15th International Workshop on the Physics of Semiconductor Devices (IWPSD)*, Dec. 2009.
6. M. Mehrad and Ali A. Orouji, *15th International Workshop on the Physics of Semiconductor Devices (IWPSD)*, Dec. 2009.
7. M. Mehrad and Ali A. Orouji, "A Novel SOI MOSFET with Buried Alumina Gate Oxide," *IEEE-RSM, Malaysia*, pp. 109-111, 2009.
8. S. Heydari, Ali A. Orouji, and M. Fathipour" *17th Iranian Conference on Electrical Engineering*, May 2009 (in Persian).
9. Zahra Arefinia and Ali A. Orouji, " *17th Iranian Conference on Electrical Engineering*, May 2009.
10. P. Razavi and Ali A. Orouji, "Improving short channel effects of sub-100nm Double gate MOSFET having high-k material in oxide stack," *14th Int. symposium on the physics of semiconductor and applications, Korea*, Aug. 2008.

11. S. Heydari, Ali A. Orouji, and M. Fathipour, "Nanoscale SOI MOSFETs with Double Step Buried Oxide: A Novel Structure for Suppressed Self-heating Effects," *International Conference on Microelectronics*, 2008.
12. P. Razavi and Ali A. Orouji, "Dual material gate oxide stack symmetric double gate MOSFET: Improving short channel effects of nanoscale double gate MOSFET," *11th International Biennial Baltic on Electronics Conference (BEC)*, pp. 83-86, Oct. 2008.
13. P. Razavi and Ali A. Orouji, "Nanoscale Triple Material Double Gate (TM-DG) MOSFET for Improving Short Channel Effects," *International Conference on Advances in Electronics and Micro-electronics (ENICS)*, pp. 11-14, Oct. 2008.
14. Ali A. Orouji, Samane Sharbati, and M. Fathipour, "A novel thin-film power MOSFET with an asymmetrical buried oxide double step structure" *6th International Conference on Electrical Engineering*, Egypt, May 2008.
15. Ali A. Orouji, *16th Iranian Conference on Electrical Engineering*, May 2008 (in Persian).
16. Zahra Arefinia and Ali A. Orouji, " *16th Iranian Conference on Electrical Engineering*, May 2008 (in Persian).
17. Samane Sharbati, Ali A. Orouji and M. Fathipour, "6H-SiC lateral power MOSFETs with an asymmetrical buried oxide double step structure," *International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, pp. 1359-1362, April 2008.
18. Ali A. Orouji and Zahra Arefinia, "The Impact of High- κ Gate Dielectrics on Carbon Nanotube Transistors," *14th International Workshop on the Physics of Semiconductor Devices (IWPSD)*, pp. 831-833, Dec. 2007.
19. Nima A. Dehdashti, Ali A. Orouji and R. Faez, "Charge Controlling in Nanoscale Shielded Channel DG-MOSFET: A Quantum Simulation," *14th International Workshop on the Physics of Semiconductor Devices (IWPSD)*, pp. 127-129, Dec. 2007.
20. Ali A. Orouji, Nima A. Dehdashti and R. Faez, "Two-Dimensional Quantum Simulation of Scaling Effects in Ultrathin Body MOSFET Structure: NEGF Approach," *14th International Workshop on the Physics of Semiconductor Devices (IWPSD)*, pp. 240-242, Dec. 2007.
21. Nima A. Dehdashti, Ali A. Orouji and R. Faez, "Full Quantum Mechanical Simulation of a novel nanoscale DG-MOSFET: 2D NEGF Approach," *IEEE AFRICON*, Sep. 2007.
22. M. Jagadesh Kumar and Ali A. Orouji, "Gate-induced Barrier Field Effect Transistor (GBFET) - A New Thin Film Transistor for Active Matrix Liquid Crystal Display Systems," *19th International Conference on VLSI Design*, pp. 89-93, Jan. 2006.
23. Ali A. Orouji and M. Jagadesh Kumar, "Analytical Modeling of Nanoscale Material Surrounding-Gate Fully Depleted SOI MOSFET," *International Conference on MEMS and Semiconductor Nanotechnology*, pp. 70-71, Dec. 2005.
24. M. Jagadesh Kumar and Ali A. Orouji, "Two-Dimensional Analytical Modeling of Nanoscale Electrically-Shallow Junction (EJ) Fully Depleted SOI MOSFET," *IEEE 16th International Conference on Microelectronics*, pp. 376-379, Dec. 2004.

25. M. Jagadesh Kumar and Ali A. Orouji, "A New Poly-Si Multiple-Gate Thin-Film Transistor (MG-TFT) with Excellent Sub-threshold Slope and Reduced Leakage Current," Accepted in *International Workshop on the Physics of Semiconductor Devices (IWPSD)*, Dec. 2005.
26. Ali A. Orouji and M. Jagadesh Kumar, "Performance Considerations of a Novel MOSFET Architecture: Symmetrical Double Gate with Electrically Induced Source/Drain," Accepted in *International Workshop on the Physics of Semiconductor Devices (IWPSD)*, Dec. 2005.
27. Ali A. Orouji and M. Jagadesh Kumar, "Electrically Shallow Junction MOSFET (EJ-SOI MOSFET)," *I² Tech Exhibition*, June 2005.
28. Ali A. Orouji and M. Jagadesh Kumar, "Shielded Channel-Double Gate (SC-DG) MOSFET," *I² Tech Exhibition*, June 2005.
29. Sara Heydari, Ali A. Orouji, " " *National Conference in Electrical Engineering*, March, 2008, Iran (in Persian).
30. Samane Sharbati and Ali A. Orouji, " " *National Conference in Electrical Engineering*, March, 2008, Iran (in Persian).
31. Reza Ghani and Ali A. Orouji, " " *National Conference in Electrical Engineering*, March, 2008, Iran (in Persian).
32. Samane Sharbati and Ali A. Orouji, " *10th Student Conference on Electrical Engineering*, Sep. 2007, Iran (in Persian).
33. Zahra Arefinia and Ali A. Orouji, "*10th Student Conference on Electrical Engineering*, Sep. 2007, Iran (in Persian).
34. Ali A. Orouji and *et al.*, "A Deep Level Transient Spectroscopy," *7th International Electrical Engineering Conference*, pp. 163-169, May, 1999, Iran (in Persian).
35. Ali A. Orouji, "Local Area Network," *8th Electrical Engineering Seminar*, pp. 6-7, Dec. 1991 (in Persian).

RESEARCH INTERESTS

- Modeling of SOI MOSFET.
- Novel Device structures.
- Analog Integrated Circuits Design.
- Shot Noise in Bipolar Transistors.

CONTACT ADDRESS

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